REMARKS

Claims 1-12 are pending in the application.

Drawing Objections

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4).

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4.) because reference characters "11 and "16 have both been used to designate first heat sink. As clearly shown in Figures 1 and 3, reference numerals 11 and 16 point to a same block.

The drawings are objected to under 37 CFR 1.83(a).

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. The Office is specifically referring to features recited in claims 6, 7 and 8.

In claim 6, the features "a space being provided in the vicinity of the junction of the first heat sink and the second heat sink, into which **an adhesive** used for joining the first heat sink and the second heat sink can flow to thereby prevent the adhesive from reaching the semiconductor light emitting element".

In claim 7, the features "at least a part of the electrode for the first-conduction-type semiconductor being in contact with the first heat sink, interposed with a **first adhesive; at** least a part of the first heat sink being in contact with the second heat sink, interposed with a **second**

adhesive; and **the total weight of the second adhesive is** twice or more heavier **than the total weight of the first adhesive".**

In claim 8, the features "the total weight of the second adhesive being five times **or more heavier than** the total weight of the **first adhesive**".

To overcome the objections to the drawings, filing concurrently herewith are the enclosed Figs. 1-3 and 5 as substitutes. In each of Figs. 1 and 3, a small drawing is added to illustrate that the first heat sink 11 is covered with the Ti/Pt/Au layer 16. The support for the amendment can be found in page 35, lines 4-7 of the present specification, i.e, "an AIN sub-mount, which entirely covered with a Ti/Pt/Au layer 16 so as to ensure the electro-conductivity in the direction of thickness, was prepared as the first heat sink 11". In this regard, please also refer to page 11, lines 10-14.

In Figs. 1-3 and 5, the numbers 15a, 15b, 15c and 15d are added instead of the number 15. The number 15a refers to the first adhesive for joining the first heat sink and the electrode for the first conduction-type semiconductor and the number 15b refers to the second adhesive for joining the first heat sink and the second heat sink. Pages 25, 28, 29, 30 and 35 of the present specification are accordingly amended. The number 15c denotes the adhesive for joining the second heat sink and the electrode for the first-conduction-type semiconductor and the number 15d denotes the adhesive for joining the second heat sink and the third heat sink. Claim 6 is supported by the paragraphs of page 28, line 16 to page 29, line 15 and the substituted Figs. 1 and 2. Claims 7 and 8 are supported by the paragraph of page 30, lines 20-32 and the substituted Fig. 1.

Objection to the Specification

The disclosure is objected to because of the following informalities: needs a detailed description of the Fig. 5. It is respectfully submitted that Fig. 5 has been amply discussed in the paragraph bridging between pages 29 and 30.

Reconsideration and withdrawal of this objection are respectfully requested.

Claim Objections

Claims 1-12 are objected to due to informality. The kind Office suggestion is adopted with appreciation.

Claim Rejections under 35 USC §112

Claim 6 is rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the present invention.

Claim 6 is amended, as needed, to overcome this rejection. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim Rejections under 35 USC §103

Claims 1, 2, 4, 5 and 10-12 are rejected under 35 USC 103(a) as being unpatentable over Hattori in view of Ochiai.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Hattori does not discloses at least a part of an electrode for the first-conduction-type semiconductor of the semiconductor light emitting element being in contact with the first heat sink, and the first heat sink and the second heat sink being in contact with each other in a junction overlooking one of the two side planes which do not compose the facets of the cavity in the semiconductor light emitting element."

The Applicant agrees with the Office assessment of the shortcoming of Hattori. The outstanding Office Action further stated that:

> "Hattori discloses in Figs. *5* and 1 OB a semiconductor light emitting device comprising:
>
> - at least one semiconductor light emitting element (7) of edge-emission type, a first heat sink (6) and a second heat sink (1),
>
> - at least a part of an electrode (19) for the second-conduction-type semiconductor of the semiconductor light emitting element (7) is in contact with the second heat sink (1)."

The Applicant respectfully disagree. It is clear that this Office Action has creatively interpreted Hattori for no other purpose than to reject the claimed invention. What the Office Action regards as a first heat sink (1) is objectively disclosed by Hattori as a guide substrate. What the Office Action regards as a second heat sink (6) is objectively disclosed by Hattori as a sub-substrate not a heat sink. The paragraph of column 5, lines 26-43 and Fig. 1 and 2 clearly indicate that the component (6) is a sub-substrate having wiring parts (10) which are electrically connected to the light-emitting diode array of an edge-emitting type (LEDA) (2) by wires (11). A person skilled in the art readily understand that the component (1) in Fig. 10B is not a heat sink, either. The paragraph of column 5, lines 26-43 and Fig. 1 clearly indicate that the component (1) is an optical-fiber-

aligning guide substrate which merely fixes the optical fibers (5) in the v-shaped grooves (4). Furthermore, the paragraph of column 9, lines 7-35 and Fig. 9B and 10B indicate that Hattori avoids contacting the light emitting part (7) with the component (1) in order to protect the light emitting part (7). Hattori does not intend that the component (1) works as a heat sink. Thus, heat sinks are not disclosed in Hattori.

What the Office Action regards as an electrode (19) for the second-conduction-type semiconductor is simply a duplication of the Applicant's own claim language, for the Office Action never identified in Hattori that there is a first-conduction-type semiconductor and a second-conduction-type semiconductor distinction; therefore, it is illogical for the Office Action to pinpoint with definitiveness that Hattori has disclosed a second-conduction-type semiconductor. The hindsight reconstruction to pick and choose among isolated disclosure in the prior art to deprecate the claimed invention is clearly exposed. In this regard, it is well settled that:

> "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

With the above-mentioned defects of the primary reference Hattori, the Office Action attempted to supplement the defects by stating that:

> "However, Ochiai disclose in Fig. 1 at least a part of an electrode for the first-conduction-type semiconductor of the semiconductor light emitting element (1) being in contact with the first heat sink (2a), and the first heat sink (2a) and the second heat sink (2b) being in contact with each other in a junction overlooking one of the two side planes

> which do not compose the facets of the cavity in the semiconductor light emitting element. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Hattori by using the first heat sink as taught by Ochiai. The ordinary artisan would have been motivated to modify Hattori in the manner described above for at least the purpose of providing a high external quantum efficiency (read PURPOSE, lines 13)."

In interpreting Ochiai, the Office Action has identified with definitiveness of a first-conduction-type semiconductor. Again, the Office is merely duplicating the language of the claimed invention rather than collecting objective disclosure of the prior art, for the Office Action has never identified a first conduction type semiconductor and a second conduction type semiconductor distinction in Ochiai.

In addition, there is simply no disclosure or teaching of at least a part of an electrode for the first-conduction-type semiconductor of the semiconductor light emitting element being in contact with the first heat sink, and the first heat sink and the second heat sink being in contact with each other in a junction overlooking one of the two side planes which do not compose the facets of the cavity in the semiconductor light emitting element.

More specifically, The Examiner states in Section 9 that Ochiai discloses in Fig. 1 that the first heat sink (2a) and the second heat sink (2b) are in contact with each other. As is clear from Fig. 1, these two heat sinks are not directly contacted with each other. The first heat sink (2a) is in contact with the glass tube (5) and the glass tube (5) is in contact with the second heat sink (2b). Since it is well known that glasses are poor heat conductors, Hattori does not intend heat conduction

from the first heat sink (2a) to the second heat sink (2b), and vice versa. It is clear that Hattori does not suggest the basic idea and the structural feature of the claimed invention.

Section 2143 of the MPEP has specifically stated that:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 466, 20 USPQ2d 1438 (Fed. Cir. 1991)"

It is respectfully submitted that the Office has not established a *prima facie* case of obviousness, because, 1) there is not any suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; 2) there is not any reasonable expectation of success in following the suggestion as stated in the outstanding Office Action; 3) the teaching or suggestion to make the claimed combination and the reasonable expectation of success cannot both be found in the asserted prior art.

For the foregoing differences, independent claim 1 patentably distinguishes over the asserted prior art. All claims dependent thereon also patentably distinguish over the asserted prior art. Reconsideration and withdrawal of this rejection are respectfully requested.

Since a *prima facie* case of obviousness has not been established in this Office Action, it would be improper for the Office to provide a new ground of rejection and make the next Office Action final, because it would effectively deny the applicant an opportunity to respond to the new ground of rejection. As an effort to assist the Office to determine whether indeed each and every element of the claimed invention is disclosed or taught in the prior art, the following claims with parenthetical blanks are submitted herewith.

1. (Amended) A semiconductor light emitting device ( ) comprising at least one semiconductor light emitting element ( ) of edge-emission type ( ), a first heat sink ( ) and a second heat sink ( ),

wherein at least a part ( ) of an electrode ( ) for a first-conduction-type semiconductor ( ) of the semiconductor light emitting element ( ) is in contact with the first heat sink ( );

at least a part ( ) of an electrode ( ) for a second-conduction-type semiconductor ( ) of the semiconductor light emitting element ( ) is in contact with the second heat sink ( ); and

the first heat sink ( ) and the second heat sink ( ) are in contact with each other ( ) in a junction ( ) overlooking one of the two side planes ( ) which do not compose facets ( ) of [the] a cavity ( ) in the semiconductor light emitting element ( ).

Claim 3 is rejected under 35 USC 103(a) as being unpatentable over Hattori and Ochiai as applied to claim 1 above, and further in view of Ishikura.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Hattori and Ochiai disclose the claimed invention except for the surface of the first heat sink which is kept in contact with the semiconductor light emitting element having an effective electro-conductivity with at least one surface which is not kept in contact with the semiconductor light emitting element."

The Applicant respectfully disagree that Hattori and Ochiai disclose the claimed invention except the noted features and elements. In fact, Hattori and Ochiai in combination contain many other defects as noted above. Therefore, even if Hattori, Ochiai and Ishikura are combined exactly as suggested in the Office Action, the claimed invention would not result.

Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 6-8 are rejected under 35 USC 103(a) as being unpatentable over Hattori and Ochiai as applied to claim 1 above, and further in view of Saito.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Hattori and Ochiai disclose the claimed invention except for a space being provided in the vicinity of the junction of the first heat sink and the second heat sink, into which an adhesive used for joining the first heat sink and the second heat sink."

The Applicant respectfully disagree that Hattori and Ochiai disclose the claimed invention except the noted features and elements. In fact, Hattori and Ochiai in combination contain many other defects as noted above. Therefore, even if Hattori, Ochiai and Saito are combined exactly as suggested in the Office Action, the claimed invention would not result.

Reconsideration and withdrawal of the rejection are respectfully requested.

Claim 9 is rejected under 35 USC 103(a) as being unpatentable over Hattori and Ochiai as applied to claim 1 above, and further in view of Oota.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Hattori and Ochiai disclose the claimed invention except for at least one of the electrodes of the semiconductor light emitting element having an Au layer having a thickness of 30 to 100 nm."

The Applicant respectfully disagree that Hattori and Ochiai disclose the claimed invention except the noted features and elements. In fact, Hattori and Ochiai in combination contain many other defects as noted above. Therefore, even if Hattori, Ochiai and Oota are combined exactly as suggested in the Office Action, the claimed invention would not result.

Reconsideration and withdrawal of the rejection are respectfully requested.

Prior Art Indicated to be Pertinent to the Disclosure

The Office has provided a list of prior art indicated to be pertinent to the Applicant's invention. Consistent with the understanding as stipulated in MPEP 706.02 that only the best prior art should be applied, this list of prior art not having been applied by the Office, it is the Applicant's understanding that the Office must have considered the listed prior art to be no more pertinent than the applied prior art of record.

CONCLUSION

Claim 1 has been amended in order to more particularly point out, and distinctly claim the subject matter to which the Applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated **August 14, 2002**.

In view of the aforementioned amendments and accompanying remarks, claim 1, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to claim 1 by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made
Request for Approval of Drawing Corrections w/Figures 1, 2, 3 and 5 marked in red ink

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/995,802

IN THE DRAWINGS:

Submitted herewith is a Request for Approval of Drawing Substitution, along with substitute drawings of Figures 1, 2, 3 and 5, as enclosed.

The applicants respectfully request that the proposed drawing substitutes submitted herewith be approved by the Examiner, and that the outstanding objection to the drawings be withdrawn.

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 25, line 4, with the following rewritten paragraph:

Now as shown in Fig. 1, by making contact between the first and second heat sinks **11,12** within a space overlooking one of the two side planes which do not compose facets of the cavity in the semiconductor light emitting element **14**, it is always ensured that the solder foil, semiconductor light emitting element **14**, first heat sink **11** and second heat sink **12** are brought into contact with each other before pressure is applied for example from the top of the first heat sink **11** and the solder material **15, 15a, 15b, 15c, and 15d** is heated to melt. This readily cancels the dimensional errors among the individual components and the element, which results in proper contact between the semiconductor light emitting element **14**, first heat sink **11** and second heat sink **12**.

Please replace the paragraphs beginning at page 28, line 16, continuing to page 29, with the following rewritten paragraphs:

As shown in Fig. 1, there is provided a space in the vicinity of the junction of the first heat sink **11** and the second heat sink **12**, into which excess solder material **15b** can preferably flow to thereby prevent such adhesive from reaching the semiconductor light emitting element **14**. More specifically, it is preferable to provide this space with no passage to the semiconductor light emitting element **14**, so that excess solder **15b** will flow into this space and there remain.

As described in the above, the thickness of the semiconductor light emitting element and thickness of the heat sink intrinsically are prone to dimensional errors, so that the mounting as illustrated in Fig. 1, in which the semiconductor light emitting element **14**, first heat sink **11** and second heat sink **12** are kept in parallel with each other, needs some mechanism by which differences of the thickness among the relevant components can be compensated for, and such relevant components can be integrated. For such purpose, it is beneficial that the thickness of the solder material **15b** is intentionally selected to be thick enough to absorb dimensional errors in the individual components, and that a certain space is provided in order to accumulate the excess, solder at a remove from the semiconductor light emitting element **14** so as to keep it contacting with the element. In the embodiment shown in Fig. 1, the solder foil is initially mounted on portion **A**, which is a part of the second heat sink, and is then melted under heating for the joining of the first heat sink **11**, second heat sink **12** and semiconductor light emitting element **14**, where a part of the solder foil flows into portion **B** of the second head sink **12**. Such space

for accommodating the solder **15b** may be recesses in the second heat sink **12**, or may be recesses in the first heat sink **11**, or may be recesses in both. While there is no limitation on the shape of the recesses, the shape is preferably such that it allows smooth flow of the solder therein and prevents reverse flow. Providing the recesses at least on a part of the second heat sink **12** is particularly preferable.

While such structural approach of providing for the solder pool is of course effective in preventing contact of the solder with the semiconductor light emitting element **14**, it is also allowable to intentionally provide on a part of the heat sink a portion capable of reducing wetting (affinity) of the solder to thereby prevent the solder **15b** for joining the first and second heat sinks **11,12** from flowing into the portion where the semiconductor light emitting element **14** is to be mounted.

Please replace the paragraphs beginning at page 29, line 34, continuing to page 30, with the following rewritten paragraphs:

The wetting (affinity) improving layer is located so as to enhance the flow of the excessive solder into the space for accommodating the solder. In particular, it is preferable to locate such layer so that the solder material **15b** will surely flow into the space while preventing flow towards the semiconductor light emitting element **14**. Specific embodiments thereof can be exemplified as those shown in Figs. 5A to 5D, other than that shown in Fig. 1. In a structure

shown in Fig. 5A, the wetting affinity improving layer is placed on a slope so that the excessive solder material **15b** can flow down leftward in the figure. In such case, the wetting (affinity) improving layer is definitely not provided in the vicinity of the top end portion of the slope, which is close to the semiconductor light emitting element **14**, so that the solder material **15b** will not flow towards the semiconductor light emitting element **14**. Also in structures shown in Figs. 5B to 5C, the device is composed so that the excessive solder material **15b** accumulates in a portion where the wetting (affinity) improving layer is formed, or flow over such portion to drop in the solder pool. Such structure may be provided in a plural number per heat sink. In such case, the individual structures may differ from each other.

In the present invention, it is preferable that at least a part of the electrode for the first-conduction-type semiconductor is in contact with the first heat sink as being interposed with a first adhesive **15a** (preferably solder material); at least a part of the first heat sink is in contact with the second heat sink interposed with a second adhesive **15b** (preferably solder material); and the total weight of the second adhesive **15b** is twice or more, and more preferably five times or more, heavier than the total weight of the first adhesive **15a**. Providing such difference in the weight of the adhesives is advantageous in that facilitating the adjustment of the semiconductor light emitting element, first heat sink and second heat sink, which should be set in parallel with each other, during the assembly.

Please replace the paragraphs beginning at page 34, line 31, continuing to page 35, with the following rewritten paragraphs:

An AlN sub-mount, having no electro-conductivity in the direction of thickness, was procured as the second heat sink **12**. The second heat sink **12** is preliminarily evaporated with a Ti/Pt/Au layer **16** on a wetting (affinity) improving layer **19**, laser mounting surface and surfaces parallel thereto in order to ensure only the conductivity within the surface, where only the laser mounting portion was further evaporated with an AuSn solder **15c** so as to be stacked on the Ti/Pt/Au layer **16**. On the other hand, an AlN sub-mount, which is entirely covered with a Ti/Pt/Au layer **16** so as to ensure the electro-conductivity in the direction of thickness, was prepared as the first heat sink **11**, where over the entire laser mounting portion an AuSn solder layer **15a** was further formed by evaporation on the Ti/Pt/Au layer **16**.

First, the semiconductor light emitting element **14** was mounted on the second heat sink **12** under the normal temperature so as to allow the n-side electrode thereof to contact with the second heat sink **12** while aligning the edge of the second heat sink **12** and the front facet of the element **14**; an AuSn solder layer of 85 μm thick is then placed on the wetting (affinity) improving layer **19**; the first heat sink **11** is positioned so that the edge thereof is recessed by 25 μm to the rear of the facet of the semiconductor laser element **14** as shown in Fig. 2; mounted to be in contact with the AuSn solder layer 85 μm thick and with a part of the p-side electrode; the temperature was raised to 290 under 30 g load, to thereby join the first heat sink **11**, second heat

sink **12** and semiconductor laser element **14** to complete a COS, the semiconductor light emitting device. In such process, excess AuSn solder was found to flow from the portions contacting the first heat sink **11** and second heat sink **12** into the area removed from both. A stem containing CuW for current injection was then prepared as a third heat sink **13**, and the COS was then joined therewith again using the AuSn solder **15d** so as to allow the bottom plane of the second heat sink **12** to contact with such third heat sink **13**. Thereafter, the portion of the first heat sink **11** covered with the Ti/Pt/Au layer **16** was bonded with three gold wires **17** of 25 μm diameter by ultrasonic fusion process to thereby produce the p-side electrode, and the second heat sink **12** covered with the Ti/Pt/Au layer **16** was also bonded with three gold wires **18** of 25 μm diameter by ultrasonic fusion process to thereby produce the n-side electrode to allow current injection. The entire structure was sealed in a nitrogen atmosphere to be completed as a can package.

IN THE CLAIMS:

Please amend claims 1 and 6 as follows:

1. (Amended) A semiconductor light emitting device comprising at least one semiconductor light emitting element of edge-emission type, a first heat sink and a second heat sink,

wherein at least a part of an electrode for [the] a first-conduction-type semiconductor of the semiconductor light emitting element is in contact with the first heat sink;

at least a part of an electrode for [the] a second-conduction-type semiconductor of the semiconductor light emitting element is in contact with the second heat sink; and

the first heat sink and the second heat sink are in contact with each other in a junction overlooking one of the two side planes which do not compose [the] facets of [the] a cavity in the semiconductor light emitting element.

6. (Amended) The semiconductor light emitting device as claimed in Claim 1, wherein a space (B) is provided in the vicinity of the junction of the first heat sink (11) and the second heat sink (12), into which an adhesive (15b) used for joining the first heat sink (11) and the second heat sink (12) can flow to thereby prevent the adhesive (15b) from reaching the semiconductor light emitting element (4).

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